



YCbCr to RGB Color Space Converter Core

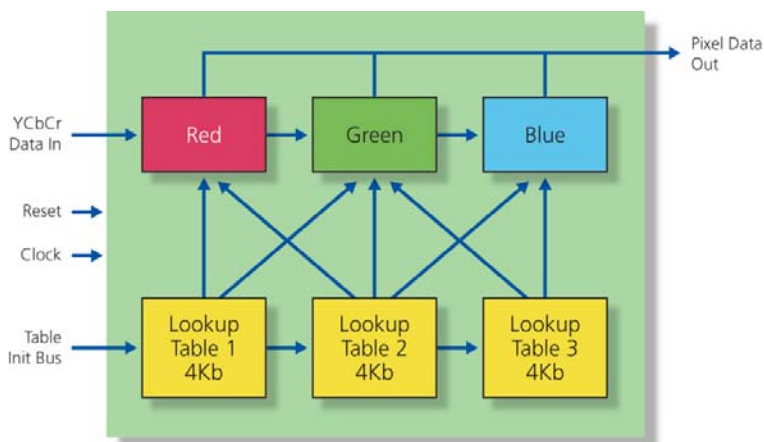
Actel
SolutionPartner

Attodyne's YCbCr to RGB Color Space Converter Core is designed for high performance and low resource utilization. This module provides a bridge between various YCbCr video sources and RGB-based LCD displays. Common YCbCr video sources include NTSC video decoders, MPEG decoders, and cameras.

Three block-RAM instances are used in place of resource-consuming multipliers and adders to implement this core. Aside from being light on resource usage, the 8-bit color-space converter is fast, reaching 90M pixels-per-second performance in a standard speed grade Actel FPGA.

A variant of this converter is available that works with mixed YCbCr/RGB data. The conversion is controlled on a pixel-by-pixel basis with an enable flag, or via one of three user-defined YCbCr windows.

Block Diagram



A 4:4:4 encoded YCbCr pixel is clocked in on each clock cycle. In pipeline-fashion, the RGB equivalent is calculated using values stored in each of the three lookup tables. If the YCbCr data happens to make excursions outside of permitted values, error detection logic compensates for these, preventing gross display artifacts.

As the designer probably knows, 4:4:4 encoded YCbCr data means that each pixel sample has color and brightness information associated with it. Most YCbCr sources are 4:2:2 encoded, indicating that color information is shared across two adjacent pixels where luminance information is unique for each pixel. It is a simple matter to convert 4:2:2 data to 4:4:4 data by reusing the color information as needed before sending the data into the color converter. However, Attodyne offers an ITU-656 interface core that performs this operation for you. In addition, it breaks out (decodes) the discrete synchronization signals as well. The latter saves I/O pins, since these signals do not have to enter the FPGA as discrete signals.

The values contained in the look up tables can be initialized by an external MCU, or by attached serial Flash. Please contact Attodyne for information about the serial Flash loading option.

Features

Maximum Pixel Clock Frequency

- >90MHz in standard speed grade FPGA

Maximum Supported Format

- Limited only by pixel clock frequency

Table Initialization Options

- External MCU
- Serial Flash

Color Depth

- 8-bit standard

Applications

- In-Car Entertainment
- Medical Imaging
- Handheld devices
- Set-Top Boxes
- Notebooks
- Kiosks
- Casino Machines
- ATMs
- POS Advertising



YCbCr to RGB Color Space Converter Core



Device Utilization

Family	Device	Tiles	Clock Globals	I/Os	PLLs	Block RAM	Utilization
IGLOO™	AGL125	269	1	78	0	3	8.8%
ProASIC®3	A3P125	269	1	78	0	3	8.8%
Fusion	AFS250	269	1	78	0	3	4.4%

Deliverables

- Complete IP Datasheet
- Actel Optimized Netlist
 - Netlist for target FPGA in EDIF, Verilog, or VHDL format
- RTL Source Code
 - VHDL or Verilog source code
 - Functional verification testbench
 - Complete Libero® Integrated Design Environment (IDE) project

About Attodyne

As an Actel Solution Partner, Attodyne licenses IP cores relating to the processing, transmission, distribution, and display of video data. Attodyne's design experience and capabilities span from ultra-low noise analog circuits to 4 Gbps fiber optic communications; however, video-related FPGA work is its primary focus. In addition to licensing IP cores, Attodyne also offers reference designs, prototypes, design consultation, and product development.

Attodyne will help guide you early in your project to extract the maximum feature set that will minimize the design cost for both hardware and firmware/software. Attodyne recommends Actel's FPGAs, as Actel's Flash based FPGA architecture is uniquely suited to video/LCD applications. Actel also provides superior support and creative flexibility to match its customer's needs. Due to a close working relationship with Actel, Attodyne has extensive knowledge of its Flash FPGAs as well as Actel's roadmap. This base of knowledge is extremely important when making long-term product and manufacturing decisions.