



Fast Video Timing Generator Core

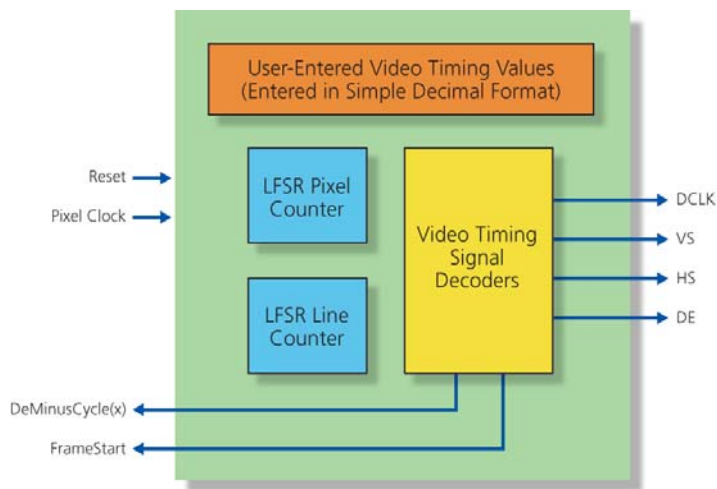


Attodyne's Fast Video Timing Generator Core (FVTG) delivers blazingly fast performance with minimum resource usage in standard speed-grade Actel FPGAs. Fixed video timing values are entered in a simplified decimal format to make setup easy.

Video timing generators create the synchronization signals required by most displays, including Display Clock (DCLK), Display Enable (DE), Vertical Sync (VS) and Horizontal Sync (HS). Additional signals queue the flow of pixel data in the rest of the system. An available ancillary module adds the additional low-level signals required by some LCD displays with a TFT-specific interface.

FVTG is a great choice when cost is a significant factor as smaller and slower speed-grade FPGAs become viable. Or, choose Attodyne's Configurable Video Timing Generator (CVTG) when the application calls for the ability to change the video format and timing on-the-fly.

Block Diagram



Features

Maximum Display Clock Frequency

- 178MHz in standard speed grade FPGA

Maximum Output Format

- 3200 total horizontal pixels
- 3200 total horizontal lines

Support Timing Signals

- Display Pixel Clock
- Display Enable
- Vertical Sync
- Horizontal Sync

System Synchronization Signals

- FrameStart – Indicates start of new frame
- DeMinusCycle(x) – A 7-bit vector that enables look-ahead view of Display Enable

Applications

- In-Car Entertainment
- Medical Imaging
- Handheld devices
- Set-Top Boxes
- Notebooks
- Kiosks
- Casino Machines
- ATMs
- POS Advertising
- Avionics
- Military

If the designer has configured the timing values for other video generating devices, he will appreciate the ease with which Attodyne's FVTG can be configured. Nearly any resolution up to 3200x3200 is supported. This is handy when driving displays with non-standard formats.

Video system designers at Attodyne developed this core in response to the need to extract maximum performance from the least amount of FPGA resources. Some of this "compact performance" is attributed to the use of advanced Linear Feedback Shift Registers (LFSRs). LFSRs are often dismissed in many applications since compare values must be derived from the desired count value via a time-consuming process. The FVTG core performs this calculation automatically at Compile time allowing the designer to take advantage of LFSR performance without having to deal with the arduous task of data conversion. The source code license for this core is almost worth the price just to see how this is done.



Fast Video Timing Generator Core



Device Utilization

Family	Device	Tiles	Clock Globals	I/Os	PLLs	Block RAM	Utilization
IGLOO™	AGL125	137	1	13	0	0	4.5%
ProASIC®3	A3P125	137	1	13	0	0	4.5%
Fusion	AFS250	137	1	13	0	0	2.3%

Deliverables

- Complete IP Datasheet
- Actel Optimized Netlist
 - Netlist for target FPGA in EDIF, Verilog, or VHDL format
- RTL Source Code
 - VHDL or Verilog source code
 - Functional verification testbench
 - Complete Libero® Integrated Design Environment (IDE) project

About Attodyne

As an Actel Solution Partner, Attodyne licenses IP cores relating to the processing, transmission, distribution, and display of video data. Attodyne's design experience and capabilities span from ultra-low noise analog circuits to 4 Gbps fiber optic communications; however, video-related FPGA work is its primary focus. In addition to licensing IP cores, Attodyne also offers reference designs, prototypes, design consultation, and product development.

Attodyne will help guide you early in your project to extract the maximum feature set that will minimize the design cost for both hardware and firmware/software. Attodyne recommends Actel's FPGAs, as Actel's Flash based FPGA architecture is uniquely suited to video/LCD applications. Actel also provides superior support and creative flexibility to match its customer's needs. Due to a close working relationship with Actel, Attodyne has extensive knowledge of its Flash FPGAs as well as Actel's roadmap. This base of knowledge is extremely important when making long-term product and manufacturing decisions.